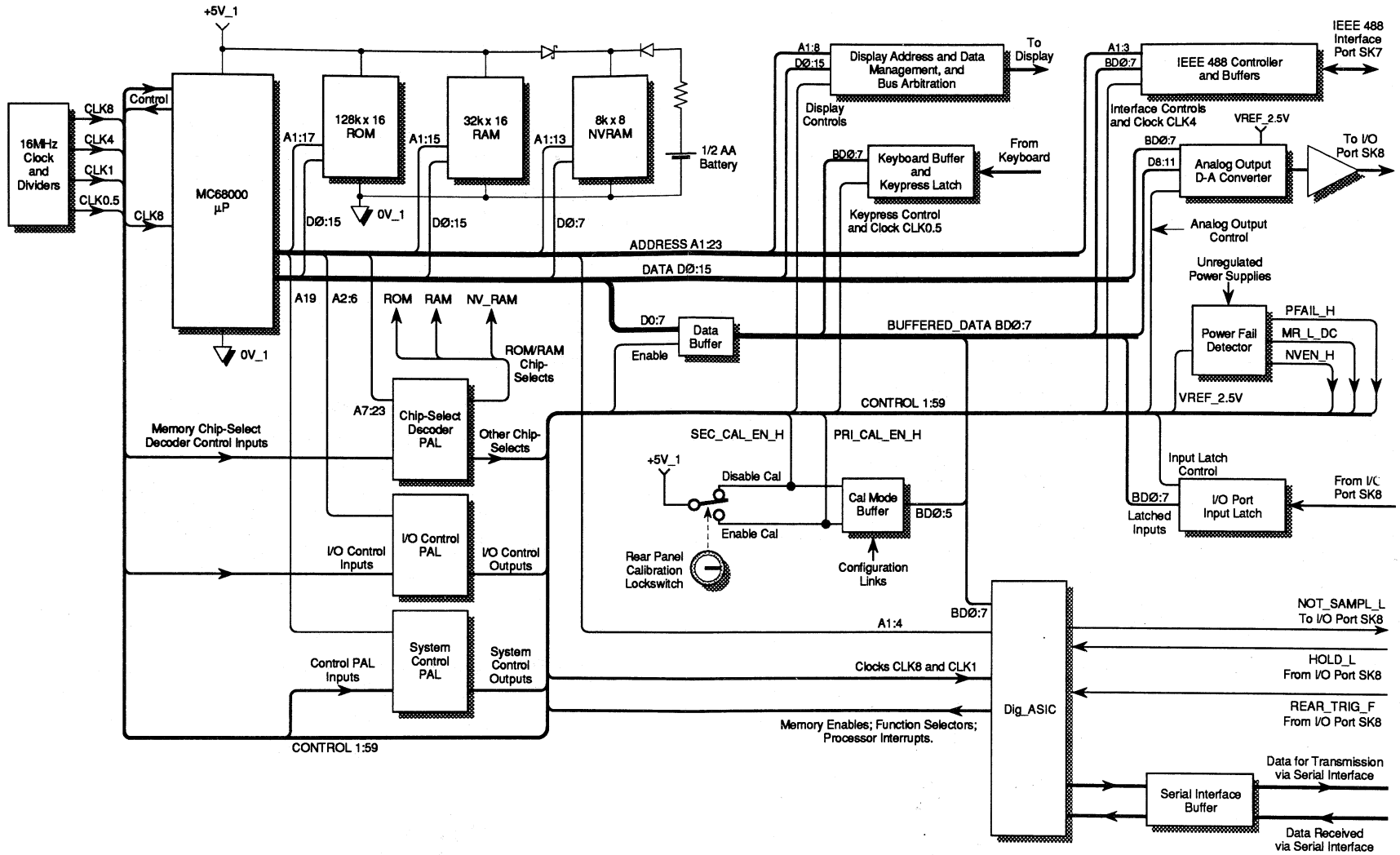

FIG. 5.2.7.1 DIGITAL PCB - MAIN FUNCTIONS

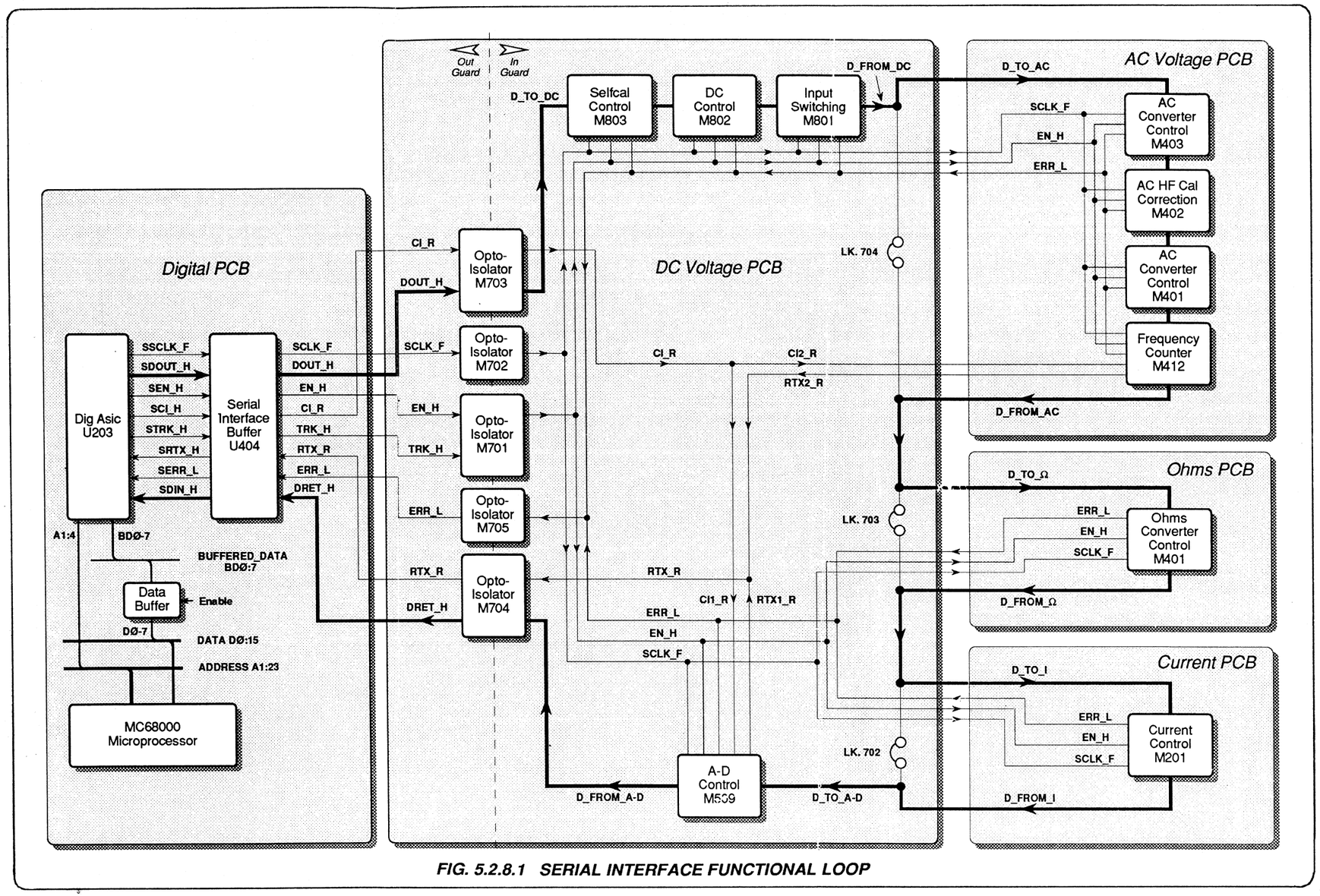

FIG. 5.2.8.1 SERIAL INTERFACE FUNCTIONAL LOOP

5.2.7.8 Analog Output

Analog output voltage is derived from measurement data stored in RAM (corrected by calibration constants). The processor writes data to the D-A convertor U205 on BDØ:7 and D8:11. Data is latched into the DAC by SEL_WORD_L (UDS_L and LDS_L combined at U111-15 *page 11.4-2*). U205 is selected by WR_DAC_L from address decoding U111-13.

When all the data is Logic-1, the Analog Output is -2.45V. All data at Logic-Ø produces +2.45V. An output of 0V is theoretically produced for inputs between hex 7FF and hex 8ØØ. In practice the output, although linear, is initially offset and requires calibration.

D201 provides a +2.45V reference to the 'R/2R' DAC. The DAC's Analog ground is connected to current mirror U206-1. U206-7 is a conventional inverting amplifier which sums the DAC output with the mirrored analog ground current from the DAC. This provides bipolar operation and output drive.

R205 protects U206-7 output, C203 and C205 prevent oscillation and D202-D205 are clamps. The Analog output is filtered by R205 and C204.

5.2.7.9 IEEE Interface

The IEEE controller (GPIA) U401 is connected to the IEEE bus via the buffers U402 and U403. Data is passed to and from the GPIA on the buffered data bus. Note that BDØ connects to D7, BD1 to D6 etc.

The GPIA is addressed via A1-A3, and runs on CLK4 to maintain bus handshake speed. It is enabled by SEL GPIA_L, derived from U111-18 *(page 11.4-2)* and read/write is selected by BR_HW_L from U107-17. LWR_L from U109-3 must also be asserted for the processor to be able to write to the GPIA.

When a valid Group Execute Trigger is received over the IEEE bus, it is transferred via the buffered data bus to U208 for decoding, then passes as GET_R from U208-16 to the digital ASIC. If triggers are allowed, CI_R is produced to initiate a measurement. Interrupts generated at U401-9 (GPIA_INT_L) are fed to the interrupt handler in the digital ASIC.

The buffers U402 and U403 are selected to Send or Receive by the GPIA U401-21. Additionally, U403 may be switched to controller mode by U401-30 (If for example there was a requirement for the 1281 to control its own 'CAL'). Special firmware would be required to employ this facility.

The GPIA has some internal de-bounce capability but extra provision has been made by fitting filter R401/C401 and R402/C402 to avoid problems which could arise due to external noise on IFC and REN.